Power Reduction & Speed Augmentation in LFSR for Improved Sequence Generator using Scaling Principle and Transistor Stacking

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Abstract - In many electronics circuit Linear Feedback Shift Register (LFSR) used for generating sequences. So for high performance applications LFSR should have to generate efficient sequences. There are so many methods of generating very efficient sequences. The demand and popularity of portable LFSR is driving designers to strive for small silicon area, higher speeds, low power dissipation and reliability. Compared to static LFSR, dynamic LFSR offers good performance. Wide fan-in logic such as domino LFSR is used in high-performance applications. Dynamic domino LFSRs are widely used in modern digital VLSI circuits. These dynamic LFSRs are often favored in high performance designs because of the speed advantage offered over static LFSR circuits. This paper compares different types of LFSR on the basis of performance parameter such as power consumption, delay, power delay product, area reduction, leakage current at 90 nm, 65 nm, 45 nm, 32 nm, and 25 nm technologies for high performance LFSR design. The techniques are compared by performing detailed transistor simulations on benchmark circuits using Microwind 3 and DSCH 3 CMOS layout CAD tools.

Key words - CMOS, Static logic, Dynamic logic, pass transistor logic, transmission gate logic, Layout, Power consumption and leakage current.

I. INTRODUCTION

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops. The aim of this paper is to compares static LFSR, domino (dynamic) LFSR and different types of LFSR which are designed by different components (Transmission gates and inverter, Pass transistors) on the basis of performance parameter such as power consumption, delay, power delay product, area reduction, leakage current at 90 nm, 65 nm, 45 nm, 32 nm, and 25 nm technologies.

II. POWER DISSIPATION

The power consumed by CMOS circuits can be classified into two categories:

A. Dynamic Power Dissipation

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are “on” simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between V_{DD} and GND and a short-circuit current flows. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behaviour of the nodes. Signals in CMOS devices transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation. [15]

B. Static Power Dissipation

This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The sub threshold leakage current increases exponentially, thereby increasing static power dissipation. [15]

- Formula for Power Dissipation:
  \[ P_d = (I_{av}) \times (V_{dd}) \]  
  Where, \( I_{av} \) = average current, \( V_{dd} \) = applied voltage.

- Formula for Leakage Current:
\[ I_{\text{leakage}} = I_0 \exp(v_{gs} - v_{th})/n\sqrt{v_t} \quad [17] \]

Here,

\[ I_0 = \mu_0 C_{\text{ox}}[W/L]\sqrt{v_t}2e^{1.8} \]

- Formula for Propagation delay:

\[ T_{pd} \alpha \left(\frac{V_{dd}}{(V_{dd} - V_{th})^2}\right) \quad [18] \]

Where,

- \( C_{\text{ox}} \) = gate oxide capacitance,
- \((W/L) = \) width to length ratio of the leaking MOS device,
- \( \mu_0 \) = zero bias mobility,
- \( V_{gs} \) = gate to source voltage,
- \( V_t \) = thermal voltage and
- \( n=2 \) (sub-threshold swing coefficient)
- \( T_{pd} = \) Propagation delay
- \( V_{dd} = \) Supply Voltage
- \( V_{th} = \) Threshold Voltage

III. PROBLEM IDENTIFICATION

For driving the MOSFET (Metal Oxide Semiconductor Field effect transistor) key parameter is the scaling of the transistor gate length, which has a significant performance impact at the 32nm node & beyond. Because of the large gate tunneling currents, the gate oxide cannot be further scaled down and beyond the 45nm node the channel length scaling without gate dielectric scaling actually degrades transistor drive current and performance.

For further reduction in scaling technology beyond the 45nm node the high-\( k \) dielectric material is introduced as gate dielectric layer. As the gate oxide thickness of a transistor reduces, performance of the transistor become poor. This will give the negative impact on all over performance of the CMOS logic circuit. For achieving this purpose semiconductor engineers have continuously decreases the thickness of the gate dielectric layer, higher leakage current will be resulted in the reduced dielectric thickness.

IV. PROPOSED METHODOLOGY

A. Scale W/L Ratio

The characteristic of MOS Device can be improved and maintained if the critical parameters of device are scaled in accordance to a given criterion. Here Fig. 1 represents basic MOS device.

If device dimension which include channel length \( L \), channel width \( W \), oxide thickness \( t_{\text{ox}} \), junction depth \( X_i \), applied voltages, and substrate concentration density \( N \) are scaled by constant parameter \( \alpha \), then the depletion layer thickness \( d \), the threshold voltage \( V_t \), and drain to source current \( I_{ds} \) are also scaled. Here Fig. 2 shows basic scaled MOS device.

The W/L ratio is very important parameter for power dissipation and leakage current of a transistor. It can be seen by the formula of current which is given by

\[ I_{\text{leakage}} = I_0 \exp(v_{gs} - v_{th}) / n\sqrt{v_t} \quad [17] \]

Here, \( I_0 = \mu_0 C_{\text{ox}}[W/L]\sqrt{v_t}2e^{1.8} \)

So if the W/L ratio scaled down then MOS device performance increased and maintained. [21]

B. Using Transistor Stack

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the “Stacking Effect” [21]. When two or more transistors that are switched OFF are stacked on top of each other [Refer Fig.10a], and then they dissipate less leakage power than a single transistor that is turned OFF [Refer Fig.3b]. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Therefore in Fig.10a transistor \( T_2 \) leaks less current than transistor \( T_1 \) and \( T_3 \) leaks less than...
T1, T2 and T3 is decreased as it flows from Vdd to Gnd. So Ileak1 is less than Ileak2. If natural stacking of transistors does not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2. The proposed D flip-flop circuit using stacking effect is shown in Fig.4. The leakage reduction achievable in a two-stack comprising of devices with widths Wu and Ws compared to a single device of width w is given by equation 5. [22]

\[
X = \frac{I_{\text{device}}}{I_{\text{stack}}} = \frac{w}{w_1} \left(1 - \frac{\lambda d}{s} \right) \left(1 - \alpha \right) \ldots(1)
\]

Where \( \alpha = \frac{1}{1 + 2 \lambda d} \ldots(2) \)

\( \lambda_d \) is the drain-induced barrier lowering (DIBL) factor and s is the sub-threshold swing coefficient. When \( w_u = w_s = w/2 \) then the leakage reduction factor or stack effect factor X is rewritten as

\[
X = \frac{w}{w_1} \left(1 - \frac{\lambda d}{s} \right) \ldots(3)
\]

\[
X = 2 \times 10^{\lambda_d V_{dd} \left(1 - \frac{1}{s} \right)} \ldots(4)
\]

\[
X = 2 \times 10^u \ldots(5)
\]

Where \( u \) is the universal two-stack exponent which depends only on the process parameter, \( \lambda_d \) and s, and the design parameter \( V_{dd} \). Thus the leakage current through a single OFF device is greater than leakage through a stack of two OFF devices.

V. EXPECTED OUTPUT

In this paper three CMOS implementations of LFSRs using static logic circuit, dynamic logic circuit, pass transistor logic circuit, and transmission gate logic circuit are proposed. This LFSR design using pass transistor logic will have the maximum delay and minimum average power. The leakage power and leakage current of all the designs will be decrease when reduction techniques will be applied. The percentage reduction of leakage power will more with the proposed scale W/L ratio technique. The design of LFSR using pass transistors with scale W/L ratio technique will gives the minimum leakage power and leakage current. The design using Transmission gate logic circuit and scale W/L ratio will gives least delay. But, if the threshold voltages of all transistors are same, then the node voltage at the end of the pass transistor chain will become one threshold voltage lower than \( V_{th} \), regardless of number of pass transistors in chain. So that due to this disadvantage of pass transistor we will use dynamic logic circuit with scale W/L ratio for designing high performance LFSR.

VI. APPLICATION

The application of LFSRs are given below

- Pseudo-noise sequences
- Fast digital counters
- Whitening sequences
- Pattern Generators
- Built-in Self-Test (BIST)
- Encryption
- Compression
- Checksums
- Pseudo-Random Bit Sequences (PRBS)

VII. CONCLUSION

On the basis of the whole performance the Pass transistor logic will have minimum power dissipation and leakage current but it cannot be cascaded with each other so that domino/dynamic logic can be used for designing high performance LFSR. From the whole system design and performance analysis it can be easy to conclude that system designed on 32nm scale will always give very high performance in comparison to other.

REFERENCES


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