Design and Analysis of Low Power Single Edge Triggered D Flip Flop

T. Ravi, Mathan.N, V. Kannan

Abstract— Low power flip-flops are crucial for the design of low-power digital systems. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are scaled down to nanometer ranges, Complementary MOS (CMOS) circuit’s total Power Consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. This fact has motivated a lot of researchers and technologists to choose leakage current minimization as their future work. Proper selection of flip-flops is necessary in order to satisfy low power and high performance circuit. In this paper investigation of conventional and proposed single edge triggered flip-flop is done with comparisons of average power, delay and power delay product which claims that proposed design is suitable for low power applications.

Index Terms— CMOS, MOSFET, Single Edge Triggered D-flip flop, Power Consumption, Delay, Power Delay Product.

I. INTRODUCTION

The system on chip (SOC) design will integrate hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat [1]. So large amount of heat should not be dissipated. Thus low power design is the need of today’s integrated systems. The low power design is also needed for the applications operated by batteries such as pocket calculators, wrist watches, mobile phones, laptops etc. It is important to prolong the battery life as much as possible. Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process shrinks according to Moore’s Law, designers are able to integrate more transistors onto the same die. The more transistors there are the more switching and the more power dissipated in the form of heat or radiation. Heat is one of the most important packaging challenges in this era; it is one of the main drivers of low power design methodologies and practices. Another mover of low power research is the reliability of the integrated circuit. More switching implies higher average current is flowing and therefore the probability of reliability issues occurring rises. The most important prime mover of low power research and design is our convergence to a mobile society. We are moving from desktops to laptops to handhelds and smaller computing systems. With this profound trend continuing, and without a matching trend in battery life expectancy, the more low power issues will have to be addressed. This entails that low power tools and methodologies have to be developed and adhered to. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today’s integrated chips.[9] In this paper the background information about flip-flop design and characteristics are analyzed.

II. BASICS OF SEQUENTIAL ELEMENTS

Sequential elements are mainly used to store computation result values for future use. At the minimal level of storage an element should be able to store a logic “1” or “0” reliably. Transitions on the inputs of a flip-flop may or may not lead to a state change. When input transitions do not change the state, the internal switching inside the flip-flop consumes some power. On the other hand, when the input transitions do change the state, a bigger amount of power is consumed. Flip-flops can be classified in several ways: dynamic vs. static, square-wave vs. pulsed, conditional vs. non-conditional, and depending on the logic style used.[20]

III. REGIONS OF FLIP-FLOP OPERATION

There are three regions of flip-flop operation, of which only one region is acceptable for a sequential design to function correctly.

The regions are:

- Stable region: Where the setup and hold times of a flip-flop are met and the Clock-to-Q delay is not dependent on the D-to-Clock delay. This is the required region of operation.
- Metastable region: As D-to-Clock delay decreases, at a certain point the Clock-to-Q delay starts to rise exponentially and ends in failure. The Clock-to-Q delay is indeterministic and this might cause intermittent failures and behaviours which are very difficult to debug in real circuits.
- Failure region: Where changes in data are unable to be transferred to the output of the flip-flop.[2]

IV. SINGLE EDGE TRIGGERED D-FLIP FLOP STRUCTURES

The simplest flip flop design is single edge-triggered, sampling data on only one clock edge (either on rising or falling clock edge). The SET flip-flops are usually configured
as Master-Slave configuration. Several single edge-triggered D flip-flop designs were proposed in the past to reduce either power or area or delay. These flip-flops are quite good at being low power and high performance.

A. POWER PC 603 SET D FLIP FLOP

The conventional SET flip flop design is shown in figure 1. It is one of the fastest classical structures and its main advantage is the short direct path and low power feedback. The large load on the clock will greatly affect the total power consumption of the flip-flop. This flip-flop is the transmission gate flip-flop, it has a fully static master–slave structure, which is constructed by cascading two identical pass gate latches and provides a short clock to output latency. It does have a bad data to output latency because of the positive setup time. And its sensitivity to clock signal slopes and data feed through is another concern when using it. [2]

![Fig.1 Power PC 603 SET D Flip Flop](image)

B. PROPOSED SET FLIP FLOP

The proposed SET D-flip flop is shown in figure 2. In many designs master slave logic is used and regenerative feedback is preferred for both master and slave. This can be modified by having regenerative feedback only for slave, which improves the efficiency. Its performance will also be more reliable than other designs. Such designs can be used for high speed applications. Modifying the existing design by changing the feedback connections in order to reduce the overall area and power consumption such that the design becomes better applicable for the low power applications.

![Fig.2 Proposed SET D Flip Flop](image)

V. SIMULATION RESULTS

To evaluate the performance, conventional and proposed flip-flop structures discussed in this paper are designed using 130-nm CMOS technology. All simulations are carried out using HSPICE simulation tool at nominal conditions with different range of frequencies from 100MHz to 1GHz. The simulated waveform of the proposed SET flip-flop is shown in Fig.3.

![Fig.3 :Transient Analysis of Proposed SET D-FF](image)

VI. PERFORMANCE ANALYSIS

The performance of the proposed SET D-FF is evaluated by comparing the average power, delay and power delay product (PDP) for conventional and proposed SET D-FF. In general, a PDP based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency. The following tables from TABLE 1 to TABLE 3 furnished the performance parameters for different range of frequencies from 100MHz to 1GHz.

<table>
<thead>
<tr>
<th>Table 1: OPERATING FREQUENCY at 100MHz</th>
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<tbody>
<tr>
<td>FLIP FLOP’s</td>
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<tr>
<td>-----------------</td>
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<tr>
<td>Power PC 603 SET D-FF</td>
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<tr>
<td>Proposed SET D-FF</td>
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<tr>
<th>Table 2: OPERATING FREQUENCY at 500MHz</th>
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<tr>
<td>FLIP FLOP’s</td>
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<td>-----------------</td>
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<tr>
<td>Power PC 603 SET D-FF</td>
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<tr>
<td>Proposed SET D-FF</td>
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</tbody>
</table>
TABLE 3: OPERATING FREQUENCY at 1GHz

<table>
<thead>
<tr>
<th>FLIP FLOP's</th>
<th>AVERAGE POWER(µW)</th>
<th>DELAY (pS)</th>
<th>PDP (aJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power PC 603</td>
<td>75.18</td>
<td>73.75</td>
<td>5540.7</td>
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<tr>
<td>SET D-FF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed SET D-FF</td>
<td>59.3</td>
<td>64.23</td>
<td>3808.8</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

In this paper, we have proposed a low power single edge triggered D flip-flop design in 130nm CMOS technology. The SET D-flip-flops are simulated with different operating frequencies ranging from 100MHz to 1GHz. The proposed SET D-Flip-flop is efficient by comparing average power, delay and power delay product. Hence by performance analysis the proposed design is efficient for low power applications.

VIII. REFERENCES

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