

High Power Amplifier designed with LDMOS: A Review

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Abstract— High Efficiency Power Amplifier for Envelope Detection is presented here in this paper which uses the LDMOS power amplifier to achieve high efficiency. The main objective in this work to design a power amplifier which is more efficient when subject to various kind of situations. QAM modulation with 64 point, and Additive White Gaussian Noise Channel was used here in this work. Amplitude Modulation, Phase Modulation response is plotted here to judge the performance of system designed. BER, MER analysis under various conditions are shown in a result.

Keywords— Base station power amplifier, digital predistortion, efficiency, envelope tracking, W-CDMA, BER, MER.

I. INTRODUCTION

As the wireless communication becomes ever more preferable, there has been an increased attention and demand for low-cost, high-efficiency, and compact systems. Among all the necessary parts involved in the wireless communication systems, RF power amplifier is known to be one of the most critical building blocks in the signal transmitters and is the most power-consuming component in the system. Thus, there has been a quite a bit of research on achieving a very efficient power amplifier.

The power amplifier (PA) is a key element in transmitter systems, whose main task is to increase the power level of signals at its input up to a predefined level. Power amplifier's requirements are mainly related to the absolute achievable output power levels. Many applications for power amplifier design are used in broadcast digital television, satellite and military system [1]. In most RF and microwave power amplifiers, the largest power dissipation is in the power transistor. Since the main power supply consumer is power amplifier, the low power feature is directly translated to power amplifier specifications. Moreover, due to the widespread diffusion of communication applications, the power amplifier designer has usually to trade-off among the contrasting goals of high transmitted power, low power consumption and highly linear operation. The resulting challenge has however heavily influenced, in the last decade, industrial, technical and research directions in the

power amplifier field. From the power amplifier designer point of view, both the selection of the active devices composing the power amplifier and especially the exploration of their non-linear operation regions, to fully exploit the output power capabilities become critical [2]. Dedicated and non linear design methodologies to attain the highest available performance become therefore crucial for successful results. Power amplifier design strongly depends on operating frequency and applications, as well as on the available device technology. For high frequency applications however, two broad power amplifier design methodologies classes are available. They are switching mode (SM) amplifier [4] and transconductance-based amplifier [5].

In general, a power amplifier uses a DC power supplied by DC supply to amplify an RF output power. Basically, a power amplifier is composed of an active device, usually a single bipolar junction transistor (BJT) or a field effect transistor (FET), DC feed, output-matching network, and input-matching network. The active device acts as a current source driven by the appropriate DC bias and the input signal. The input and output matching networks optimizes the source and the load to the transistor impedances to provide maximum gain. The overall efficiency of the transistor is defined as the ratio of RF power received by the load to the DC power fed into the amplifier. On top of the efficiency measurement of the power amplifier, another important parameter for high efficient power amplifier is power added efficiency (PAE). Power added efficiency is a measurement of maximum output RF power to input RF power over the DC power fed into the amplifier. Thus, it is important to be able to transfer the maximum amount of DC power to the load as RF power.

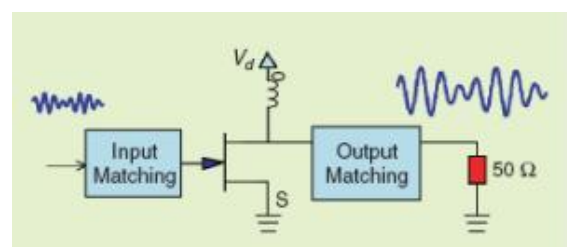


Figure 1. Basic Topology of Power Amplifier

The figure above shows the basic topology of a power amplifier. As the figure shows, the power amplifier is composed of four most important components: DC feed through RF Choke, transistor, input matching network, and output matching network. It is the designer's choice to choose the type of transistor and to design input and output matching networks according to the applications. For Class-F power amplifiers, many researches have been done focusing on the output matching network. As indicated earlier, Class-F amplifiers use harmonic resonators at the drain of the transistors to trap infinite number of harmonics to eventually eliminate the overlap between the voltage and the current waveforms. However, due to increased components and increased parasitic considerations, many current theories only consider second and third harmonics.

II. ENVELOPE TRACKING BASE STATION AMPLIFIER

The traditional approach to linearly amplify the nonconstant envelope modulated signal is to "back off" the linear Class-A or Class-AB PA's output power until the distortion level is within acceptable limits. Unfortunately, this lowers efficiency significantly, especially for high PAR signals. Thus, there is an inherent tradeoff between linearity and efficiency in PA design. A block diagram of the EER systems is shown in Fig. 2.

The highly efficient envelope amplifier is critical to the EER system since the total system efficiency is the product of the envelope amplifier efficiency and RF transistor drain efficiency.

The block diagram of the envelope tracking amplifier used in this work is shown in Figure 3. The W-CDMA signal is generated in the digital domain, and consists of an envelope signal, as well as I and Q RF signals. Care has been taken to ensure the proper spectral mask and a reasonable peak to average ratio (7.6 dB), which includes a dcresting algorithm as well as a circularity algorithm for measurement consistency. After up-conversion, the resultant RF signal provides the input to the RF amplifier, whose supply voltage is modulated by the amplified envelope signal by the wide band and high efficiency envelope amplifier. To minimize distortion by the time delay difference between envelope and RF path, synchronization is performed by comparing the input and down-converted output signal [6].

Pre-distortion is also carried out in the digital domain in order to minimize the AM-AM and AM-PM distortion caused by the RF amplifier and envelope amplifier. Dcresting (an adjustment of the peak-to-average ratio), is performed digitally on the envelope of the signal to optimize the efficiency, ACLR and EVM performance. To avoid gain collapse of RF amplifier at low drain voltages, the envelope of the signal is also dcrestoughed (adjustment is made to the envelope signal in the vicinity of its zeros). This technique

has been used with a number of devices and a number of modulated signals [6,7].

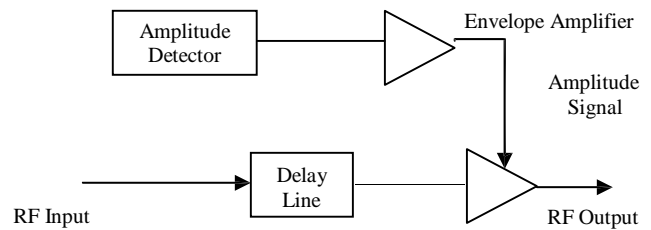


Fig 2. EER System

Wide Band High Efficiency Envelope Amplifier used in this work, which is shown in Figure 4, comprises a linear stage to provide a wide band voltage source and, in parallel, a switching stage to provide an efficient current supply. The output voltage of the envelope amplifier follows the input envelope signal with help of an operational amplifier. The current is supplied to the drain of RF amplifier from both the linear stage and the switching stage through the current feedback which senses the current flowing out of the linear stages and turns on/off the switch [8].

The linear stage provides the difference between the desired output current and the current provided by the switching stage, such that the overall error is minimized. This V_{dd} amplifier is being used for a wide range of applications, resulting in a slight reduction in efficiency.

Measurement of the high voltage envelope amplifier used in this work shows average drain efficiency around 64% with a W-CDMA signal, a peak drain voltage of 29.4 V, an RMS (root-mean-square) value of 12.4 V. Therefore, it is suitable for the base station power amplifier using high breakdown voltage LDMOS devices. The efficiency of the V_{dd} amplifier could be improved by selecting components that are more precisely selected for this application.

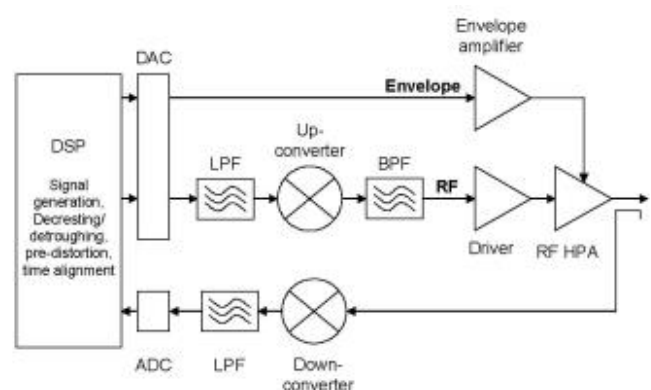


Fig 3. Base Station High Power Amplifier

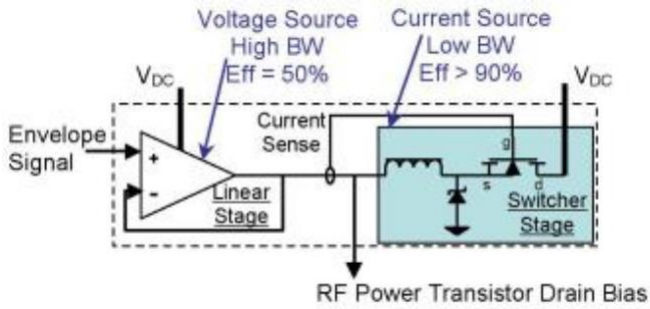


Fig 4. Wide Band High Efficiency Envelope Amplifier.

III. TRANSISTOR POWER AMPLIFIER

A general definition of the implementation may be found under the heading or term AM Receiver which contains an overview.

1) Common Base Envelope Detector

The term amplifying detector is used in this case, because the circuit is both an envelope detector and an amplifier. Of course the diode detector used in the previous example would not be considered an amplifier.

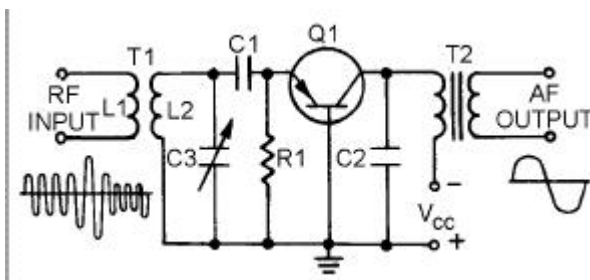


Fig 5. Common base envelope detector

The amplitude modulated RF input is applied to the primary [L1] of transformer T1.

The Emitter-Base junction forms an equivalent diode detector as covered before. The Collector side of the transistor serves as the amplifier section, so the circuit is the same as a diode detector followed by an amplifier. The input section comprised of T1 and capacitor C3 form a tuning circuit which is adjusted to the frequency of the incoming modulation envelope. [or its center frequency]. The adjustable capacitor is used to tune the LC circuit [C3 & L2] to the desired frequency.

Resistors R1 and C1 only serve to bias the transistor and set the DC bias point of the Emitter circuit. R1 provides the DC bias; however the combination of R1 and C1 act as a filter producing a varying DC voltage to the input of the transistor. The voltage resulting from the filter follows the rises and falls

of the incoming envelope. The varying dc bias on the Emitter junction causes an identical, but amplified, voltage on the Collector of the transistor.

The detected envelope which happens to be the desired Audio Frequency [AF] is passed to the output. The Collector voltage is applied to the transistor through the output transformer [T2]. The primary of T2 forms the load of the transistor. Capacitor C2 is an RF bypass capacitor. The load of the circuit segment is the transformer, but the ultimate output is connected to the secondary of T2 and not shown.

2) Common Emitter Envelope Detector

An alternative circuit to detecting the envelope of an AM signal is shown below. This circuit approach uses a Common-Emitter transistor configuration. The term common-emitter detector might be used to describe the circuit. Common Emitter refers to the fact the Emitter leg of the transistor is common to both the input circuit [Base-Emitter] and the output circuit [Collector-Emitter].

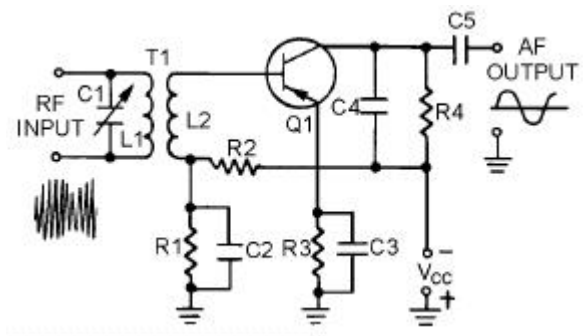


Fig 6. Common-Emitter Envelope Detector

As before the amplitude modulated input is applied to transformer T1. However this time the tuned circuit [C1 & L1] is found on the primary of the transformer. The adjustable capacitor is tuned to the desire frequency of the modulated wave [audio frequency]. The transformers secondary couples the signal to the Base of the transistor. Resistors R1 and R2 form a voltage divider which supply a DC bias to the Base of the transistor. Capacitor C2 [and C3] is a bypass capacitor which shorts out resistor R1 for RF signals.

The Emitter-Base junction of the transistor acts as the detection diode. The incoming voltage is developed across R1, of the R1/R2 voltage network. The varying [AF] frequency voltage is applied to the Base of the transistor and amplified by the Collector circuit.

The output signal is developed across resistor R4, which again is bypassed for RF by capacitor C4. Capacitor C5 is simply a DC blocking capacitor which blocks the DC voltages [Vcc] needed by transistor Q1 to function from reaching the next circuit down the line.

IV. CONCLUSION AND FUTURE WORK

Various schemes for the use of Power amplifier in WCDMA has been reported in this review paper. A brief review of various schemes has been tested over MATLAB 7.8.1, the future work can be done by increasing the capacity of HPA, and their generalise use for WCDMA using VLSI methods.

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